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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,203	02/10/2005	Hiroaki Ozeki	MAT-8657US	9927
23122	7590	03/17/2009		
RATNERPRESTIA P.O. BOX 980 VALLEY FORGE, PA 19482			EXAMINER TIMORY, KABIR A	
			ART UNIT 2611	PAPER NUMBER
			MAIL DATE 03/17/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/524,203

Applicant(s)

OZEKI ET AL.

Examiner

KABIR A. TIMORY

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

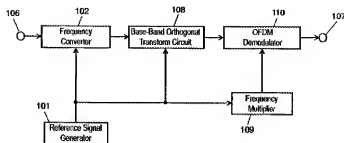
1. This office action is in response to the amendment filed on 02/26/2009. Claims 1-10 are pending in this application and have been considered below.
2. Applicant arguments regarding the rejection under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Takahashi et al. (US 5732068) have been fully considered but they are **not persuasive**. The examiner thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meets the claimed limitation as rejected.

Applicant's argument: "Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:
... a frequency multiplier wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier ...".

Examiner's response: In figure 5 below, the applicant disclose a conventional digital receiver (Applicant's Admitted Prior Art (AAPA)). In this figure the AAPA shows a

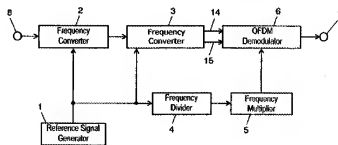
frequency multiplier 109 which outputs an output signal to the OFDM modulator 110 (see figure 5 below).

FIG 5



In figure 1, the applicant discloses a digital receiver according to an embodiment of the instant application, as shown below:

FIG 1

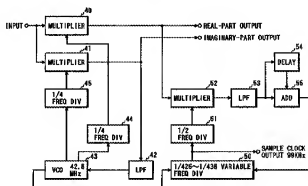


Comparing these two figures, it is clear that the only difference between the two figures is the frequency divider 4 that is added at the input of the frequency multiplier 5 of the digital receiver as shown figure 1 above. Since the multiplier 109 of AAPA and the multiplier 5 of the instant application are similar multiplier; therefor, it is obvious the multiplier 109 of AAPA has a "multiplicand value".

In figure 6 below, Takahashi et al. disclose a frequency divider 51 at the input of the multiplier 52. The output of the divider 51 is applied to the input of the multiplier 52

as shown in figure 6 below. This is the same operation as is disclosed by the applicant in figure 1 above. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider 109 as taught by Takahashi et al. and modify the system of AAPA by including the multiplier 109 of Takahashi et al. at the input of the multiplier 109 of the AAPA. By doing so, we can multiply the "multiplicand value" of the multiplier 109 and the divided frequency of the divider 52 in order to produce a desired input signal by for the OFDM modulator 110 of the AAPA.

FIG. 6



Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (figure 5, specification, page 1, lines 10-27, and page 2, lines 1-2) in view of Takahashi et al. (US 5732068).

Regarding claim 1:

As shown in figure 5, AAPA a digital signal receiver comprising:

- a reference signal generator (101 in figure 5) for generating a first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2);
- a base band transform circuit (108 in figure 5) for converting a first high-frequency signal with digital modulation into a base band signal with using the first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2); and
- a digital demodulator (110 in figure 5) to demodulate a signal output from the base band transform circuit with using the signal output from the frequency multiplier as a reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2);
- wherein the first reference signal is generated independent of the signal output of the frequency multiplier (signal generator of figure 5 (AAPA) illustrates the same configuration as figure 1 and 3 of the instant application. Therefore, the examiner is interpreting that the first reference signal is generated independent of the signal output of the frequency multiplier) (101 in figure 5).

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a frequency divider to divide a frequency of the first reference signal; a frequency multiplier wherein an output frequency of the frequency multiplier is

a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier.

However, Takahashi et al. in the same field of endeavor teaches a frequency divider (51 in figure 6) to divide a frequency of the first reference signal (figure 6 clearly shows that the divider 51 divides the frequency output from variable frequency divider 50 by half); a frequency multiplier (52 in figure 6) wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier (col 11, lines 61-67, col 12, lines 1-31). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Takahashi et al. to modify the system and method of (AAPA) in order to produce an error signal for the system.

Regarding claim 2:

AAPA et al. further discloses a frequency converter (102 in figure 5) for receiving a second high-frequency signal modulated by the digital signal and converting a frequency of the second high-frequency signal to generate the first high-frequency signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 3:

AAPA et al. further discloses wherein the frequency converter converts the second high-frequency signal into the first high-frequency signal with using the first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 4:

AAPA et al. further discloses wherein the first high-frequency signal is modulated by the digital signal by Orthogonal Frequency Division Multiplexing system (110 in figure 5), and the digital demodulator comprises an Orthogonal Frequency Division Multiplexing demodulator (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 5:

AAPA et al. further discloses wherein the base band transform circuit comprises an orthogonal base band transform circuit (108 in figure 5) operable to convert the first high-frequency signal into a first base band signal and a second base band signal orthogonal each other and output the first base band signal and the second base band signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 6:

AAPA et al. further discloses wherein the orthogonal base band transform circuit includes a 90°-phase shifter for shifting a phase of the first reference signal by 90 degrees (base-band orthogonal transform circuit is interpreted to generate signal which are shifted 90 degree from each other such as I and Q signal) (108 in figure 5), a first mixer (102 in figure 5) for mixing the first reference signal with the first high-frequency signal to convert the first high-frequency signal into the first base band signal, and a second mixer (108 in figure 5) for mixing the second reference signal with the first high-frequency signal to convert the first high-frequency signal into the second base band signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 7:

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a device including the frequency divider and at least one of the base band transform circuit and the frequency converter.

However, Takahashi et al. in the same field of endeavor teaches a device including the frequency divider (51 in figure 6) and at least one of the base band transform circuit (see figure 6) and the frequency converter (40 and 41 in figure 6). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Takahashi et al. to modify the system and method of (AAPA) in order to produce an error signal for the system.

Regarding claim 8:

AAPA et al. further discloses a device including the digital demodulator (110 in figure 5) and the frequency multiplier (109 in figure 5).

Regarding claim 9:

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a low-pass filter for receiving a signal output from the frequency divider and outputting a signal to the frequency multiplier.

However, Takahashi et al. in the same field of endeavor teaches a low-pass filter (37 in figure 1) for receiving a signal output from the frequency divider (35 in figure 1) and outputting a signal to the frequency multiplier (53 in figure 1). Although, in figure 6, Takahashi et al. shows that the LPF 53 is located after the multiplier 52, however, it

would have been obvious to one of ordinary skilled in art to locate the LPF between the multiplier 52 and divider 51 in order to yield predictable result and pass only components of the output signal of the divider 51 which correspond to a divided frequency effective in frequency control. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Takahashi et al. to modify the system and method of (AAPA) in order to produce an error signal for the system.

Regarding claim 10:

(AAPA) further discloses a further device including the digital demodulator (110 in figure 5) and the frequency multiplier (109 in figure 5).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **KABIR A. TIMORY** whose telephone number is (571)270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kabir A Timory/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611